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### **AMENDMENTS TO THE CLAIMS**

This listing of claims will replace all prior versions, and listings, of claims in the application:

### **LISTING OF CLAIMS:**

Claim 1 (canceled).

Claim 2 (currently amended): The integrated circuit package according to claim 43, wherein said semiconductor die is a micro electro-mechanical system integrated circuit chip.

Claim 3 (currently amended): An integrated circuit package comprising:  
a substrate having conductive traces therein, the substrate including a  
cavity therein;  
a semiconductor die mounted to a first surface of the substrate, in a flip-  
chip orientation such that a sensor portion of said semiconductor die is aligned with said  
cavity and conductive interconnects connect pads of the semiconductor die to said  
conductive traces of said substrate;  
an underfill material surrounding said interconnects;  
a plurality of conductive balls disposed on said first surface of said  
substrate, said conductive balls being electrically connected to said conductive traces  
such that ones of said conductive balls are connected to ones of said pads of said  
semiconductor die via said conductive traces; and ~~The integrated circuit package~~  
~~according to claim 1, further comprising~~  
an overmold material covering a back side of said semiconductor die and  
said plurality of conductive balls such that portions of said conductive balls are exposed,

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Claim 4 (original): The integrated circuit package according to claim 3, further comprising a plurality of second level interconnects connected to the exposed portions of ones of said conductive balls.

Claim 5 (currently amended): The integrated circuit package according to claim 43, further comprising a lid disposed on a second surface of said substrate and covering said sensor portion of said semiconductor die.

Claim 6 (currently amended): The integrated circuit package according to claim 43, wherein said underfill comprises a polymeric encapsulant.

Claim 7 (currently amended): The integrated circuit package according to claim 43, wherein said sensor portion of said semiconductor die is exposed to air.

Claim 8 (currently amended): The integrated circuit package according to claim 43, wherein said sensor portion of said semiconductor die is covered with a polymeric material.

Claim 9 (canceled).

Claim 10 (currently amended): The process according to claim 911, wherein mounting said semiconductor die comprises mounting a micro electro-mechanical system integrated circuit chip.

Claim 11 (currently amended): A process for fabricating an integrated circuit package, comprising:

providing a substrate having conductive traces therein, the substrate including a cavity therein;

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mounting a semiconductor die to a first surface of the substrate, in a flip-chip orientation such that a sensor portion of said semiconductor die is aligned with said cavity and conductive interconnects connect pads of the semiconductor die to said conductive traces of said substrate;

filling an area surrounding said interconnects with an underfill material;

mounting a plurality of conductive balls on said first surface of said substrate and in electrical connection with said conductive traces such that ones of said conductive balls are connected to ones of said pads of said semiconductor die via said conductive traces; and ~~The process according to claim 9, further comprising~~

overmolding using an overmold material to cover a back side of said semiconductor die and said plurality of conductive balls such that portions of said conductive balls are exposed.

Claim 12 (original): The process according to claim 11, further comprising mounting a plurality of second level interconnects to the exposed portions of ones of said conductive balls.

Claim 13 (currently amended): The process according to claim 9~~11~~, further comprising mounting a lid on a second surface of said substrate such that said lid covers said sensor portion of said semiconductor die.

Claim 14 (currently amended): The process according to claim 9~~11~~, wherein filling an area surrounding said interconnects with an underfill material comprises filling said area with a polymeric encapsulant.

Claim 15 (currently amended): The process according to claim 9~~11~~, further comprising singulating said integrated circuit package from a remainder of a strip of gang-fabricated packages.

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Claim 16 (currently amended): The process according to claim 911, wherein said mounting the semiconductor die includes locating the conductive interconnects on to the semiconductor die and then attaching the die to the corresponding conductive pads on the substrate.